## REMARKS

Claims 1-13, 20, and 31-41 are currently pending in the application. Claims 8-12, 14-19, 21-30, and 32-41 were withdrawn from consideration by the Examiner as being directed to a non-elected invention or species. By this amendment, claims 14-19 and 21-30 are canceled as directed to a non-elected invention. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

***Allowable Subject Matter***

Applicants appreciate the indication that claims 2-7 contain allowable subject matter. However, claims 2-7 are not being presented in independent form at this time, because Applicants submit that all of the pending claims are in condition for allowance for the following reasons.

In response to the Statement of Reasons for Allowance provided in the Office Action, Applicants wish to clarify the record with respect to the basis for the patentability of claims in the present application. In this regard, while Applicants do not disagree with the Examiner's indication that certain identified features are not disclosed by the references, Applicants submit that each of the claims in the present application recite a particular combination of features, and that the basis for patentability of each of these claims is based on the totality of the particular features recited therein.

***35 U.S.C. §102 Rejection***

Claims 1, 13, 20, and 31 were rejected under 35 U.S.C. §102(b) for being anticipated by U.S. Patent Application Publication No. 2001/0003364 issued to Sugawara et al. ("Sugawara"). This rejection is respectfully traversed.

To anticipate a claim, each and every element as set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. MPEP §2131. Applicants submit that the references supplied by the Examiner do not show each and every feature of the claimed invention.

The present invention relates to a method of (and a substrate for) manufacturing strained and non-strained silicon regions on the same chip. It is known to impart tensile or compressive stress to semiconductor devices to improve device performance. Such stresses may be imparted by forming the devices in areas of strained silicon. However, imparting these stresses may lead to defects in the areas of strained silicon. Defects can be detrimental in that they degrade the performance of defect-sensitive devices (e.g., DRAM devices), and compromise the production yield of defect sensitive devices. Exemplary implementations of the invention avoid such detrimental effects by allowing high-performance logic devices to be made in strained regions of a chip and high-quality, defect-sensitive devices to be made in non-strained regions of the same chip. Independent claim 1 recites, in pertinent part:

> 1. A method, comprising:
> forming a pattern of strained material and relaxed material on a substrate;
> forming a strained device in the strained material; and
> forming a non-strained device in the relaxed material.

Independent claim 31 recites:

> 31. An electrical device, comprising:
> a pattern of strained material and relaxed material formed on a substrate;
> a first device formed in the first strained material; and
> a second device formed in the relaxed material.

Sugawara does not disclose these features. The Examiner asserts that Sugawara shows these features in FIG. 1 (noting items 1a and 1b). Applicants respectfully disagree.

Sugawara shows a semiconductor device having an n-type device 15a and a p-type device 15b, both devices 15a, 15b constituting strained devices formed in strained material. The n-type 15a device is formed atop a silicon layer 7a that is provided on a relax layer 3. The mismatch between the silicon layer 7a and the relax layer 3 causes the silicon layer 7a to become strained. Thus, the n-type device 15a is a strained device formed on strained material. The p-type device is formed atop a silicon layer 7b that is provided on a SiGe compound layer 6. The silicon layer 7b becomes stressed due to the mismatch between the silicon layer 7b and the SiGe compound layer 6. Thus, the p-type device 15b is also a strained device formed on strained material. Moreover, Sugawara explicitly teaches that both the n-type device 15a and the p-type device 15b are formed on strained areas of silicon. Specifically, in Paragraphs [0049] and [0050], Sugawara states:

> [0049] In the nMOSTr 15a, since the silicon layer 7a is provided on the relax layer 3 made from the silicon-germanium compound whose stress is relaxed because it is formed on the buffer layer 2, **tensile stress is generated in the silicon layer 7a, so that the mobility of electrons is increased by the strain effect due to tensile stress in the silicon layer 7a.** As a result, the operational speed of the nMOSTr 15a in which the source/drains regions 13a are formed in the silicon layer 7a is improved.

> [0050] On the other hand, in the pMOSTr 15b, since the silicon-germanium compound layer 6 is provided on the silicon substrate 1, **compressive stress is generated in the silicon-germanium compound layer 6, so that the mobility of positive holes is increased due to the strain effect due to the compressive stress in the silicon-germanium compound layer 6**. As a result, the operational speed of the pMOSTr 15b in which the source/drain regions 13b are formed in the silicon-germanium compound layer 6 is improved.

As is clear from the above-noted passages, both of the devices 15a and 15b are formed on strained silicon, and no device is formed in relaxed material. Thus, Sugawara does not disclose: forming a non-strained device in relaxed material, as recited in claim 1; or a device formed in relaxed material, as recited in claim 31. To the contrary, both of the Sugawara devices 15a and 15b are formed on areas of strained silicon, and neither device 15a, 15b constitutes a non-strained device formed in relaxed material. Therefore, Sugawara does not contain each and every feature of the claimed invention, and does not anticipate the claims.

Applicants submit that claims 13 and 20 depend from allowable claim 1, and are allowable at least for the reasons discussed above with respect to claim 1. Moreover, the applied art does not disclose the features additionally recited in these claims. In fact, the Examiner admits that Sugawara does not disclose the features recited in claims 13 and 20, and, instead, asserts that the claimed features are inherent in Sugawara.

More particularly, the Examiner asserts that layer 7b is inherently doped with Ge atoms diffusing from SiGe layer 6 during the formation of the source and drain regions 13b. Applicants respectfully disagree. The Examiner is reminded of the following guidance that MPEP §2112 provides regarding inherency:

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of

> that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).
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> ...
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> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original)

Applicants respectfully submit that the Examiner's reasoning does not adequately establish that layer 7b is necessarily doped with Ge atoms diffusing from SiGe layer 6 during the formation of the source and drain regions 13b. In fact, Applicants submit that the Examiner's reasoning is mere speculation, and respectfully request that documentary evidence be provided supporting the assertion if the rejection is to be maintained.

Accordingly, Applicants respectfully request that the §102(b) rejection of claims 1, 13, 20, and 31 be withdrawn.

***Request for Rejoinder of Withdrawn Claims***

Applicants request that the Examiner rejoin claims 8-12 and 32-41 and examine these claims on the merits. As discussed above, generic claim 1 is allowable, thus rejoinder and

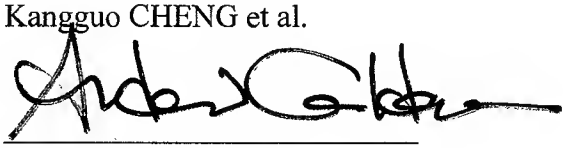
examination of claims 8-12 is proper. Also, because linking claim 31 is allowable for the reasons set forth above, rejoinder and examination of claims 32-41 is proper.

Moreover, as claims 8-12 and 32-41 depend from allowable independent claims, Applicants believe that these claims are patentably distinct from the applied prior art and are in condition for allowance.

## CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0458

Respectfully submitted,
Kangguo CHENG et al.



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